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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,472	07/23/1999	RETO STAMM	X-528-US	4229

24309 7590 10/03/2002

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/360,472	Applicant(s) Stamm et al.
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 27, 2002* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct. 25, 1999* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office action is response to applicant's amendment filed on June 27, 2002 to the related patent application S/N: 09/360,472. Claims 1-20 are pending in this official action.

Drawings

1. The drawings filed on Oct. 25, 1999 are formally accepted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dockser et al., patent no. 5,963,454.

As per claim 1, Dockser anticipated method and system for designing complex function cores in an integrated circuit by compilation and synthesis with feature representation very identical to the claimed invention (Abstract). According to Dockser, the design method includes steps of generating a set of parameter values for the logic cores (Figs. 1B, 4, "Disclosure of the Invention", col. 4) wherein the parameters would take randomly generated values for design

change or modification, for example (col. 2, lines 44-59, col. 12), generating a netlist file for circuit design, and simulating the circuit behavior (Fig. 1B, cols. 6-8) for design verification.

As per claim 2, Dockser anticipated parameter values are randomly generated and bounded in a selected range values (col. 7, lines 25-49).

As per claim 4, Dockser anticipated user interface for input data values (col. 6, lines 21-44,).

As per claims 3, and 5-17, Dockser anticipated design parameter values are randomly generated for logic core design for design modification (col. 2, lines 44-59), and design values are alternatively changed to meet design criteria, including permuting parameter variables, modifying parameters, etc. (Col. 2, lines 44-59, col. 8, line 56 to col. 9, line 32, for example), wherein the permutation would allow user to mutate parameters and randomly take values to reflect a change in design or modification of the design (col. 2, lines 44-59).

As per claim 18, Dockser anticipated system for testing and verifying logic circuit design, including a controller configured to generate design parameter variables, a logic core generator for generating netlist of the design from the logic core and design parameter variables, a logic simulator for simulating the design as claimed (Figs. 1B, 4, Background of the Invention, col. 4, col. 6, lines 52-63, col. 8, lines 24-34, col. 8, line 56 to col. 9, line 32, for example).

As per claim 19, in addition to limitations as shown in claim 18, Dockser also anticipated graphic user interface for designer (col. 6). Thus, claim 19 is rejected in like manner.

As per claim 20, Dockser anticipated system for designing complex function cores in an integrated circuit by compilation and synthesis with feature representation very identical to the

claimed invention (Abstract). According to Dockser, the design system includes means for randomly generating a set of parameter values for the logic cores (Figs. 1B, 4, "Disclosure of the Invention", col. 4), a netlist file generator for generating circuit design connection file, and simulating the circuit behavior (Fig. 1B, cols. 6-8) for design verification.

Response to Arguments

4. Applicant's arguments filed June 27, 2002 have been fully considered but they are not persuasive.

In response to applicant's argument Dockser does not disclose randomly generating a set of parameter values (page 2, paragraph 1), the examiner disagrees with. Dockser discloses parameters files are generated and input of generated parameter values are used for testing and simulating integrated circuit. Parameter values are generated and checked for correct ranges (col. 7, lines 9-24, col. 8, line 35 to col. 9, line 32). Due to design alterations or design changes, design parameter values would be randomly generated as needed (col. 2, lines 44-59, col. 12, lines 1-65) and such design modification, alteration or change would require design parameters randomly generated to reflect such change.

In response to applicant's argument Dockser fails to teach generating a random parameter value (page 3, paragraph 2), the examiner disagrees with. Parameter values are generated and checked for correct ranges (col. 7, lines 9-24, col. 8, line 35 to col. 9, line 32). Due to design alterations or design changes, design parameter values would be randomly generated as needed (col. 2, lines 44-59, col. 12, lines 1-65) and such design modification, alteration or change need

to be randomly generated to such change, e.g., bus bandwidth change, RAM type, processor architectures, etc. (col. 7, line 60 to col. 10).

In response to applicant' argument Dockser fails to teach assigning probability to one or more number between upper and lower limits (page 3, paragraph 30), the examiner disagrees with. Dockser discloses parameter values are generated and to account for design change or modification it would necessarily require the randomness of parameter values. In other word, randomness would take a distribution function or probability function as claimed such that the generation of parameter values would be typically feasible and meet design environment.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Patent no. 6,212,667 B1, issued to Geer et al., on Apr. 2001

2. Patent no. 6,243,851 B1, issued to Hwang et al., on June 2001

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for Formal communications; please mark "EXPEDITED PROCEDURE"),

Or:

(703) 746-7239 (for Unofficial Fax communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

September 30, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER